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EXAMINER	
NGUYEN, STEVE N	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,606	PLUNKETT, DOMINIC	
	Examiner	Art Unit	
	Steve Nguyen	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *14-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are currently pending.

Election/Restrictions

2. Applicant's election without traverse of Group I, claims 1-13 in the reply filed on 9/11/2006 is acknowledged. Claims 14-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 9/11/2006.

Drawings

3. The drawings are objected to because Fig. 2 does not contain descriptive labels for any of the blocks. It is suggested that descriptive labels be provided to at least some of the blocks in Fig. 2 as done in Fig. 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 3 objected to because of the following informalities: the word "list" is missing from "connections list". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 2 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites, "to identify whether, for a given pin, a BSDL file is present and whether the given pin is connected through the netlist to a pin of a device for which a BSDL file is present".

It is unclear what is meant by a given pin being "connected through the netlist" because a netlist is only a representation of the connections in a circuit and does not physically make the connections.

It is assumed that the "given pin" referred to above is a pin of a device. Therefore in the limitation, "whether the given pin is connected through the netlist to a pin of a device for which a BSDL file is present" it is assumed that the "pin of a device for which a BSDL file is present" refers to another pin (other than the "given pin"). However, it is unclear if that other pin is from the same device or not.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Folea, Jr. (US Pat. 6,988,229; hereinafter referred to as Folea) in view of Beausang et al (US

Pat. 6,012,155, hereinafter referred to as Beausang). Note: IEEE 1149.1 is brought in as a teaching reference in claims 5 and 13 to further show features of Folea, which adopts the standard.

As per claim 1:

Folea teaches circuit testing equipment comprising:

- a computer having stored thereon a boundary scan description language (BSDL) file (col. 4, lines 31-41); and
- a connector for connecting the computer to a boundary scan bus of a circuit to be tested (col. 3, lines 59-63);
- the computer being arranged to parse the BSDL file (col. 4, line 56) and generate a data structure therefrom which, when combined with a test script, permits execution of the test script from the computer through the boundary scan bus (col. 5, lines 7-19).

Not explicitly disclosed by Folea are a netlist and a connections list. However, Lulla teaches a boundary-scan capable circuit that controls a circuit that is not boundary-scan capable (col. 2, lines 54-59). Tiong in an analogous art teaches a simplified method of creating BSDL and netlist files (col. 3, lines 26-31).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to test the apparatus of Lulla in the test system of Folea by using the system of Tiong to generate BSDL files of boundary-scan capable circuit 102 and netlist files of non-compliant JTAG circuit 104. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because

one of ordinary skill in the art would have recognized that the system of Folea could test the circuit of Lulla and that the method of Tiong simplifies the BSDL and netlist generation process (col. 3, lines 11-15).

As per claim 2:

Folea further teaches the equipment of claim 1, wherein the computer has all information necessary to identify whether, for a given pin, a BSDL file is present and whether the given pin is connected through the netlist to a pin of a device for which a BSDL file is present, whereby the pin can be controlled using the boundary scan bus (col. 4, lines 35-41; complete BSDL information is provided in the system).

As per claim 3:

Folea further teaches the equipment according to claim 1, wherein the computer comprises a parser for parsing the BSDL file, the netlist and the connections, and a compiler for compiling the same to generate the data structure for execution with the test script (col. 4, lines 56-67).

As per claim 4:

Folea further teaches the equipment according to claim 1, wherein the computer further comprises at least one test script for testing an integrated circuit of the circuit to be tested (col. 5, lines 38-42).

As per claim 5:

Lulla further teaches the equipment according to claim 1, for testing a circuit that has at least one boundary-scan capable IC (col. 2, lines 55-56), the at least one boundary-scan capable IC having at least a first pin and a second pin (Fig. 1, elements

116 and 120), wherein at least the first pin is capable of adopting one of three states, being a high state, a low state and an input state (pin 120 is an input pin).

Not explicitly stated is the equipment further comprising connection test software arranged to test that the first and second pins are not connected, by setting the first pin to the input state and driving the second pin sequentially into the high and low states. However, IEEE 1149.1 teaches that the boundary scan register allows testing for short circuit connections between pins (page 60). Therefore, it would have been obvious to test the connection between two pins as suggested by IEEE 1149.1.

As per claim 6:

Folea further teaches the equipment according to claim 1, wherein the computer further comprises a first test script for testing a first integrated circuit of the circuit to be tested and a second test script for testing a second integrated circuit of the circuit to be tested (col. 5, lines 20-25; the system has a test script for any number of circuits).

As per claim 7:

Lulla further teaches the circuit testing equipment according to claim 1 for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable (col. 2, lines 55-56) and at least one second IC that is not boundary-scan capable (col. 2, lines 56-57), wherein the data structure defines all pins of the first IC that are capable of driving pins of the second IC (pins 116, 120, 124, 128, and 132 are driver pins; see Table 1) and all pins of the first IC that are capable of reading pins of the second IC (data is read through pin 120), whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC (col. 1, lines 46-47).

As per claim 8:

Folea teaches circuit testing equipment for testing a circuit, the equipment comprising:

- an input for inputting files comprising a boundary scan description language (BSDL) file (col. 4, lines 31-41); and
- a data structure generated from the BSDL file (col. 5, lines 7-19),

Not explicitly disclosed by Folea is at least one first integrated circuit (IC) that is boundary-scan capable, and at least one second IC that is not boundary-scan capable; and netlist and connections list that defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC.

However, Lulla teaches at least one first integrated circuit (IC) that is boundary-scan capable (col. 2, lines 55-56), and at least one second IC that is not boundary-scan capable (col. 2, lines 56-57); and pins of the first IC that are capable of driving pins of the second IC (pins 116, 120, 124, 128, and 132 are driver pins; see Table 1) and all pins of the first IC that are capable of reading pins of the second IC (data is read through pin 120), whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC (col. 1, lines 46-47). Tiong in an analogous art teaches a simplified method of creating BSDL and netlist files (col. 3, lines 26-31).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to test the apparatus of Lulla in the test system of Folea by

using the system of Tiong to generate BSDL files of boundary-scan capable circuit 102 and netlist files of non-compliant JTAG circuit 104. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the system of Folea could test the circuit of Lulla and that the method of Tiong simplifies the BSDL and netlist generation process (col. 3, lines 11-15).

As per claim 9:

Lulla further teaches the equipment according to claim 7 wherein the first IC has pins that are capable of adopting one of three states, being a high state, a low state and an input state (pin 120 is an input pin).

As per claim 10:

Folea further teaches the equipment according to claim 7 wherein the first IC is connected to a boundary scan bus (Fig. 1, element 125).

As per claim 11:

Folea further teaches the equipment according to claim 7, further comprising a parser and a compiler for parsing and compiling the BSDL file, the netlist and the connections list to generate the data structure, wherein the parser and compiler are implemented in computer programs loaded into a computer to be connected to the circuit to be tested (col. 4, lines 56-67).

As per claim 12:

Folea further teaches the equipment according to claim 11, wherein the computer further comprises a test script for testing the second IC and its connections to the first IC (col. 5, lines 29-41; a scan operation tests connections between circuits).

As per claim 13:

Lulla further teaches the equipment according to claim 8, wherein the at least one first IC has at least a first pin and a second pin (Fig. 1, elements 116 and 120), wherein at least the first pin is capable of adopting one of three states, being a high state, a low state and an input state (pin 120 is an input pin).

Not explicitly stated is the equipment further comprising connection test software arranged to test that the first and second pins are not connected, by setting the first pin to the input state and driving the second pin sequentially into the high and low states. However, IEEE 1149.1 teaches that the boundary scan register allows testing for short circuit connections between pins (page 60). Therefore, it would have been obvious to test the connection between two pins as suggested by IEEE 1149.1.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steve Nguyen
Examiner
Art Unit 2138

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